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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,689	05/21/2001	Thomas Grey Beutler	00CXT0074C	8701

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EXAMINER	
JAMAL, ALEXANDER	

ART UNIT	PAPER NUMBER
2643	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,689	BEUTLER ET AL.	
	Examiner	Art Unit	
	Alexander Jamal	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Based upon the amendment submitted 9-9-2004, examiner withdraws the 35USC 103 rejections to claims 2-31 of Scott et al. (5870046) in view of Staffiere (6137671).

2. The examiner provides two new sets of rejections (in the same manner as presented in the previous office action), the first of Staffiere (6137671) to claims 1,7, and the second of Scott et al. (5870046) in view of Ozawa et al. (5172304) in view of Bora (4761881) to claims 1-31.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. **Claims 1,7** rejected under 35 U.S.C. 102(e) as being anticipated by Staffiere (6137671).

As per **claim 1,** Staffiere discloses a capacitive structure (Fig. 15) comprising electrode 640 disposed on the first side of the substrate 650, and electrode 660 disposed on a second side of the substrate. The Substrate functions as a dielectric between the electrodes (Col 7 lines 48-64). He further discloses that the electrodes may be embedded within or on the surface (of either side) of the substrate (Col 8 lines 17-25). The structure further comprises first circuitry 700 coupled to one electrode 640, and second circuitry 690 coupled to electrode 660 with the use of a via. Both the first and second circuitry are on one side of the substrate.

As per **claim 7,** Staffiere discloses a multi-layer circuit board (Fig. 15: Col 7 lines 48-64) with a plurality of substrates (comprising materials 620,650 in Fig. 15).

Claim Rejections - 35 USC § 103

5. **Claims 1-31** rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (5870046), and further in view of Ozawa et al. (5172304).

As per **claim 1,** Scott discloses a high voltage isolation barrier structure (Abstract) comprising first and second electrodes (Capacitor 209 Fig. 2) with one elctrode coupled to line side circuitry and the other coupled to system side circuitry. However, Scott does

not disclose forming the capacitor by disposing the first electrode on a first side of a circuit board substrate and the second electrode on the second side of the substrate so that the substrate between the electrodes acts as a dielectric material for the capacitive structure. Furthermore, Scott does not disclose that first and second circuitry are located on the same side of the substrate used to form the embedded capacitor, with one electrode of the capacitor coupled to the first circuitry (system side circuitry in the DAA of Scott), and the second electrode coupled to the second circuitry (line side in the DAA of Scott).

Ozawa discloses that the creation of a capacitor embedded within a printed circuit board can allow the designer to embed capacitors within a pcb (multiplayer substrate) or any assembly for which the board may be placed in (Col 1 lines 10-55). He further discloses a capacitive structure (Fig. 2) comprising an electrode 4 disposed on the first side of the substrate 2, and electrode 4 disposed on a second side of the substrate. The Substrate functions as a dielectric between the electrodes (Col 3 lines 10-33). He further discloses that the electrodes may be embedded within or on the surface (of either side) of the substrate (Col 1 lines 40-55). It would have been obvious to one of ordinary skill in the art at the time of this application to implement the isolation barrier capacitors within the printed circuit board for the purpose of reducing the required circuit board surface area and allowing ease in selecting capacitor values over a wide range.

Bora teaches that components mounted on PCB's require a soldering process that adds cost, and chances for defects in the manufacturing process. Bora teaches the motivation to reduce cost from the manufacturing process (BORA: Col 1, lines 50-68). Bora also discloses that PCB's with components mounted on both sides require additional

steps (and hence additional cost) to solder on (BORA: Col 3 line 18 to Col 4 line 10). Furthermore, Ozawa teaches that one of the concepts of his invention is that the capacitors and their adjacent components (such as resistors) may be arranged so as to minimize the trace length (to improve high frequency characteristics). He also discloses an embedded capacitor in (OZAWA: Fig. 3, Col 1 lines 53-68) with coupling plates on opposite sides of the substrate. Furthermore, in the case that the line and system circuitry are on the same side, the PCB inherently comprises a via for the purpose of coupling components on opposite sides of the substrate. It would have been obvious to one of ordinary skill in the art at the time of this application to perform a design tradeoff analysis (cost versus high-frequency response) and either arrange the line and system side circuitry (or any portions thereof) on either a single side of the substrate (to save manufacturing costs) or on both sides of the substrate (to improve high frequency response by connecting a portion of the line side circuitry as closely to one of the coupling plates and a portion of the system side circuitry as closely to the other one of the coupling plates on the opposite side) for the purpose of optimizing the high frequency performance or manufacturing cost.

As per **claim 8,** claim rejected for the same reasons as the rejection of claim 1.

As per **claim 19,** claim rejected as a method performed by the system in the rejection of claim 1.

As per **claim 29,** claim rejected for same reasons as rejection claim 1. Additionally, Scott discloses a data access arrangement for a modem (Abstract, Col 1

lines 36-47) comprising a computer system. A modem is inherently used in a computer system for the purpose of having the computer system interacting with and providing/retrieving data to/from the modem. A computer system inherently comprises a data bus for the purpose of transporting data to various locations within the computer system. A computer system inherently comprises a processor coupled to the data bus for the purpose of managing and processing the data being transported on the data bus. The modem is inherently coupled to the data bus of the computer for the purpose of transmitting/receiving data to/from the processor and rest of the computer system. The system also comprises capacitor 209 (Fig. 2) with two electrodes. Capacitor 209 (Fig. 2) has system side circuitry 225 coupled to the first electrode and line side circuitry 226 coupled to the second electrode (Col 8 lines 29-43). In Scott's data access arrangements (in Figs. 2 and 7), the system side circuitry can communicate with the host system and the line side circuitry can communicate over a telephone network as described in (Fig. 1: Col 6 line 56 to Col 7 line 20).

As per **claim 2,** in Scott's high voltage isolation barrier, capacitor 209 (Fig. 2) has system side circuitry 225 coupled to the first electrode and line side circuitry 226 coupled to the second electrode (Col 8 lines 29-43).

As per **claim 3,** Scott discloses a data access arrangement (Scott: Col 8 lines 29-43) comprising isolation capacitor 209 implemented on the circuit board taught by Ozawa.

As per **claims 4/5,** Scott discloses a data access arrangement comprising isolation capacitor 209 implemented on the circuit board taught by Ozawa and contained within a modem (Col 1 lines 36-47). A modem is inherently used in a computer system for the purpose of having the computer system interacting with and providing/retrieving data to/from the modem.

As per **claim 6,** with Scott's isolation capacitors implemented on a circuit board as taught by Ozawa, the circuit board will comprise radio frequency circuitry (Scott: Col 11 lines 40-57). The 100pF value of the capacitors are radio frequency circuitry, as well as the processing circuitry in system side circuitry 225 and line side circuitry 226 (Scott: Fig. 2).

As per **claims 7,16,23,** Ozawa discloses a multi-layer circuit board (Fig. 3: Col 3 line 60 to Col 4 line 12) with a plurality of substrates.

As per **claim 9,** in Scott's data access arrangements (in Figs. 2 and 7), the system side circuitry can communicate with the host system and the line side circuitry can communicate over a telephone network as described in (Fig. 1: Col 6 line 56 to Col 7 line 20).

As per **claim 10,** in Scott's data access arrangement, capacitor 209 (Fig. 2) provides high voltage isolation between the system and line side circuitry (Col 7 lines 60-64).

As per **claims 11,22,** in Ozawa's circuit board, the electrodes of the embedded capacitor are substantially overlapping (Fig 3).

As per **claim 12,25,** claims rejected for same reasons as claim 1 rejection.

As per **claims 13,26,** Ozawa discloses that the electrical conductor (which forms the first and second electrodes in Fig. 3) can be made from copper (Col 3 lines 20-30).

As per **claim 14,** in Scott's data access arrangement, the data and control information (clock signal) are communicated between the system and line side circuits in a serialized digital format via the capacitor (Col 4 lines 30-44).

As per **claim 15,** in Scott's data access arrangement, there is one additional capacitor 210 (Scott: Fig. 2) coupled between system side circuitry 225 and line side circuitry 226. Ozawa further discloses another embodiment in Fig. 5, with a first and second capacitor formed with the substrate between each set of electrodes.

As per **claim 17,24,31,** in Ozawa's circuit board (Fig. 3), the first electrode 4 would be formed on multiple substrates (on either side of substrate 6) when implemented in Scott's system. The first electrode would comprise the electrode plus a coupling path (via) to another substrate layer (Col 3 line 60 to Col 4 line 12) to couple to circuitry on the surface of the PCB.

As per **claims 18,27,** Ozawa discloses that the electrodes (conducting layers) are printed on the substrate by a screening process (Col 3 lines 10-50).

As per **claim 20,** in Scott's method, the first and second communication circuits (as described in the rejection of Claim 19), along with the isolation capacitors form a portion of a data access arrangement (ABSTRACT).

As per **claims 21,30,** in Scott's data access arrangement, capacitor 209 (Fig. 2) provides high voltage isolation between the system and line side circuitry (Col 7 lines 60-64).

As per **claim 28,** in Scott's data access arrangement, the data and control information (clock signal) are communicated between the first and second communication circuits via the capacitor formed within the circuit board (Col 4 lines 30-44).

Response to Arguments

6. Applicant's arguments with respect to the claim 1-31 rejections have been considered but are moot in view of the new ground(s) of rejection shown above.

7. Applicant's arguments regarding the declaration filed to overcome the Staffiere reference have been fully considered but they are not persuasive. 37 CFR 1.131 part b states:

"The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application. **Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence satisfactorily explained.**"

No exhibits, drawings or records, or photocopies have been received.

Response to Declaration

8. Examiner has noted the Declaration filed May 19, 2004 under 37 CFR 1.131. It has been considered but is ineffective to overcome the Staffiere reference. The evidence submitted is insufficient to establish applicant's alleged actual reduction to practice of the invention in this country or a NAFTA or WTO member country after the effective date of the Staffiere reference. Supporting documents should be provided.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 703-305-3433. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 703-305-4708. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9315 for After Final communications.

AJ
January 13, 2005

HUYEN LE
PRIMARY EXAMINER